

BlueGene/L Project status

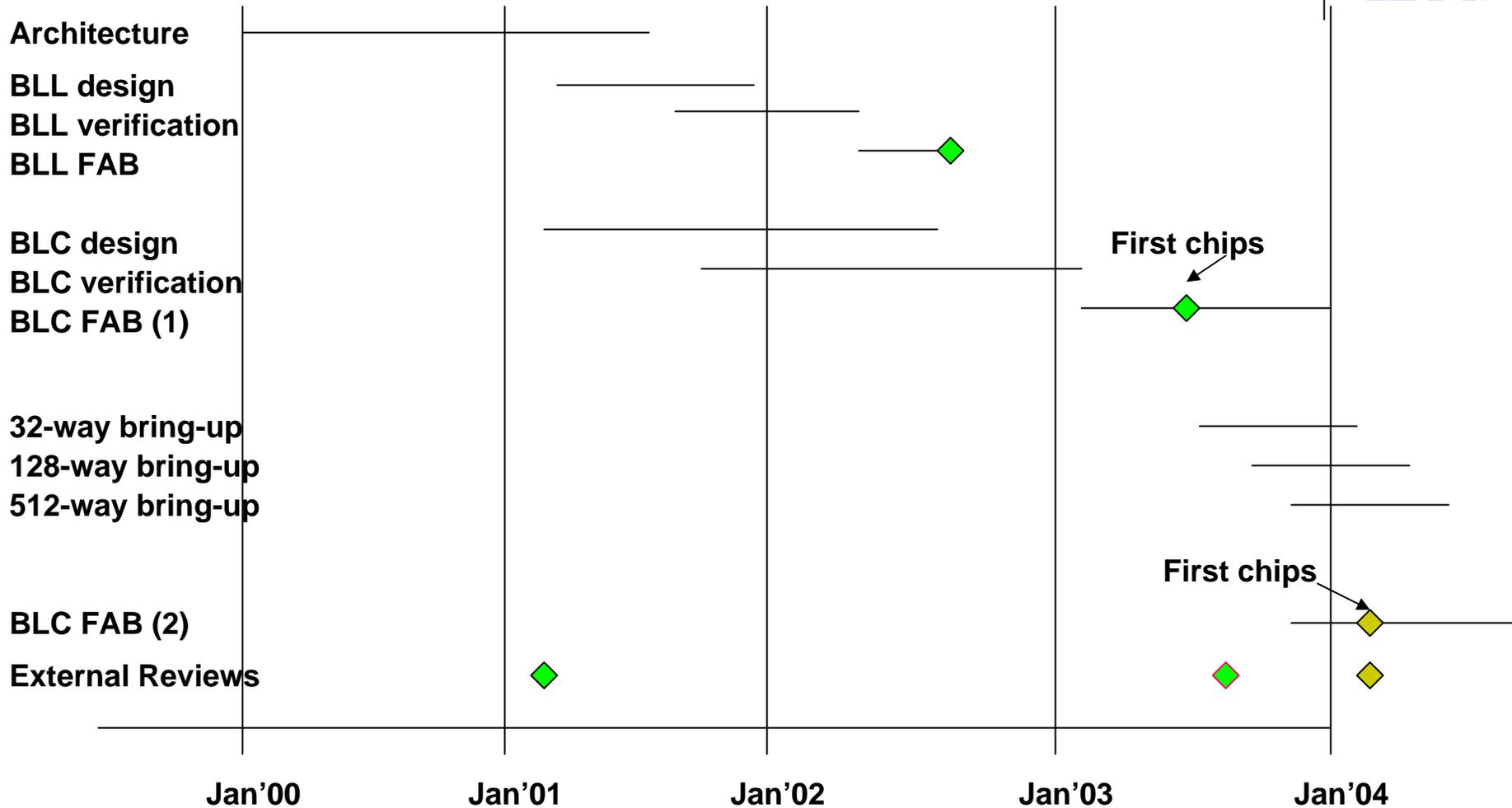
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BlueGene/L Project History





Bring-up Team Leaders

Overall: Al Gara

Torus: Phil Heidelberger

Tree : Burkhard Steinmacher-Burow

Memory: Martin Ohmacht

Links: Gerry Kopcsay

Testint : Ruud Haring

Packaging: Paul Coteus

Host: Dong Chen

System Software: Jose Moreira

Apps: Blake Fitch / Gyan Bhanot

FPU: Jim Sexton



Bring-up Responsibilities

- Pre-Hardware
 - Develop tests to cover hardware
 - Functional Path
 - Error Path
 - Performance Test Cases
- Post-Hardware
 - Execute tests on hardware
 - Scale tests as hardware scales
 - Investigate unexpected behavior through enhanced tests and simulation when necessary
 - Develop aggressive exercisers which do rare things often.
 - Inject errors where possible (links, memory)
- Prepare for next chip release
 - Characterize issue and determine appropriate logic change
 - Create simulation test case to verify change



Bring-up status

- We have successfully scaled to 512 node
- Problems identified
 - Timing problems
 - Clock tree limits chip frequency to about 75% of design
 - High speed torus and tree links vulnerable to clock domain-domain jitter. (Two of the torus links and one of the tree)
 - Various other non-critical problems
 - Simplify software
 - Increase system robustness
 - Increase self test capabilities
- Dynamics look clean
 - No Torus network routing / deadlock problems
 - No Tree network routing / deadlock problems
 - We have made a change to correct a potential live-lock situation not seen in hardware.
 - No Memory system problems of any type
 - No FPU logic problems found
- Optimistic that next chip is logically clean.