Intel Fast Forward Processor and Memory
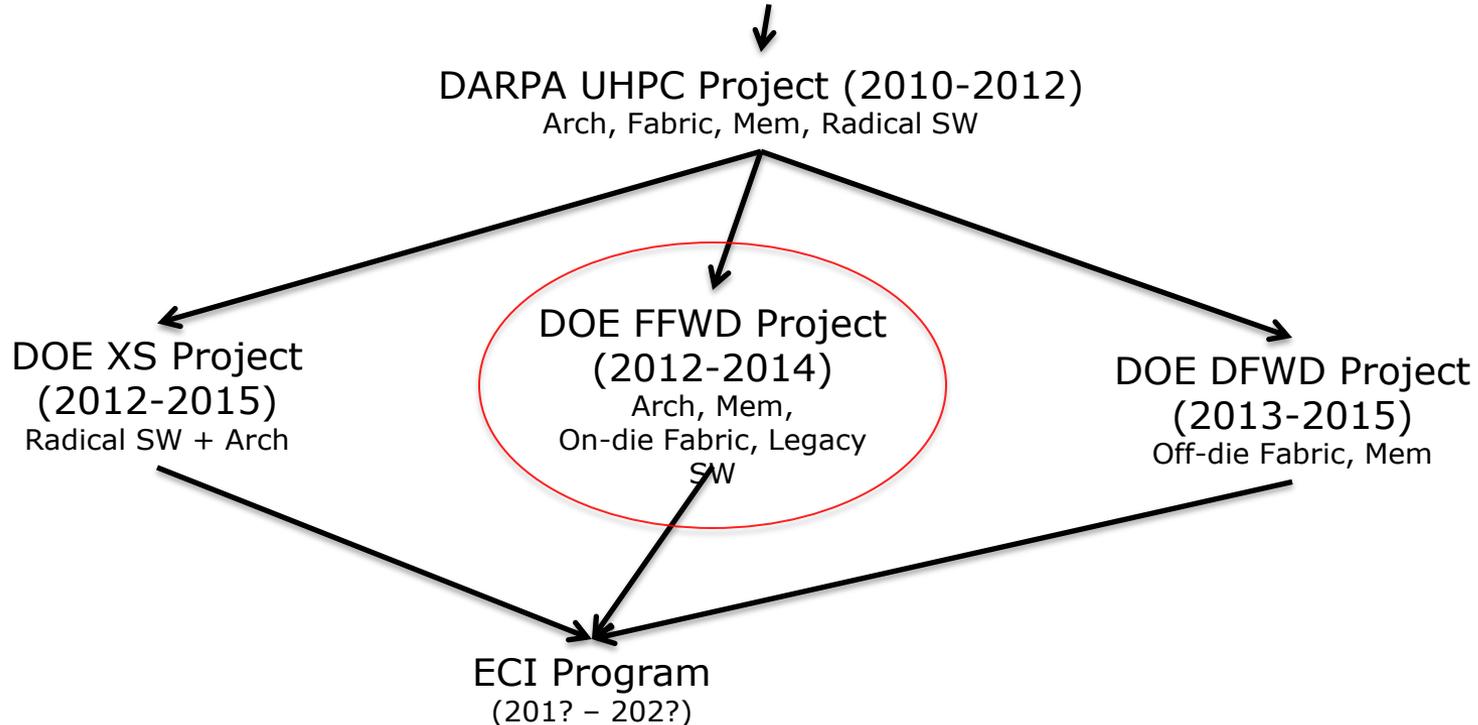
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The Challenge

- 1 DP ExaFLOP (1018 DP FLOP/sec) in 20 MW
  - This is ~20 pJ/Op at system level with all taxes; compute ~5 pJ

DARPA and DOE ExaScale Studies (pre-2010):

DARPA UHPC Project (2010-2012)
Arch, Fabric, Mem, Radical SW

DOE XS Project
(2012-2015)
Radical SW + Arch

DOE FFWD Project
(2012-2014)
Arch, Mem,
On-die Fabric, Legacy
SW

DOE DFWD Project
(2013-2015)
Off-die Fabric, Mem

ECI Program
(201? – 202?)

Top Exascale Challenges

- System Power & Energy
- Efficient, memory subsystems
- Extreme parallelism, data locality, gentle-slope programmability
- New execution model comprehending self awareness with introspection
- Resiliency to provide system reliability

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Top Exascale Challenges

- Intel's FFWD:

- System Power & Energy

- Efficient, memory subsystems

- Extreme parallelism, data locality, gentle-slope programmability

- New execution model comprehending self awareness with introspection

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Exascale Architecture Thesis Position

- System view: Energy is king, communication is queen
  - These will make or break the system
- Small simple cores
  - Efficiency and scalability vs IPC limitations
- State management, relaxed ordering, hybrid coherence
  - Limit coherency support, no large-regions of ccSM
  - Inject relaxed memory models, totally visible state
- Prioritize small comms/synch instead of ST/vector perf
  - Strong scaling is a power and cost imperative
  - Dedicate area to efficient (power and latency) comms helpers
- Pay the cost of resiliency on remote operations
  - Confirm comms to recover from remote faults/failures
  - Develop protocols (SW and HW) to quarantine errors, limit ripples
- Make it fractal
  - Same trade-offs apply in hierarchal fashion to entire system
  - Tapering is required in the hierarchy even with over-provisioning

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Intel's FFWD Elements

- Core Architecture Processor defined
  - Large number of energy-efficient cores (processing elements PE)
  - With dedicated support units to off-chip interfaces
- Software Tools and Applications are provided:
  - Architecture is exercised in a full execution-driven parallel functional simulator that itself is a parallel application
  - Allows functionality, timing, and energy estimation
  - Compiler toolchain and runtime environment
  - Focus on the six 6 DOE FFWD mini-apps, but prepare for more complex applications
- Design and Implementation: Architecture is captured in RTL:
  - Provides area and power estimates
  - Is a key software development vehicle for ongoing research
  - Prepares for the fabrication of a future silicon test chip

FFWD Processor microarchitecture overview
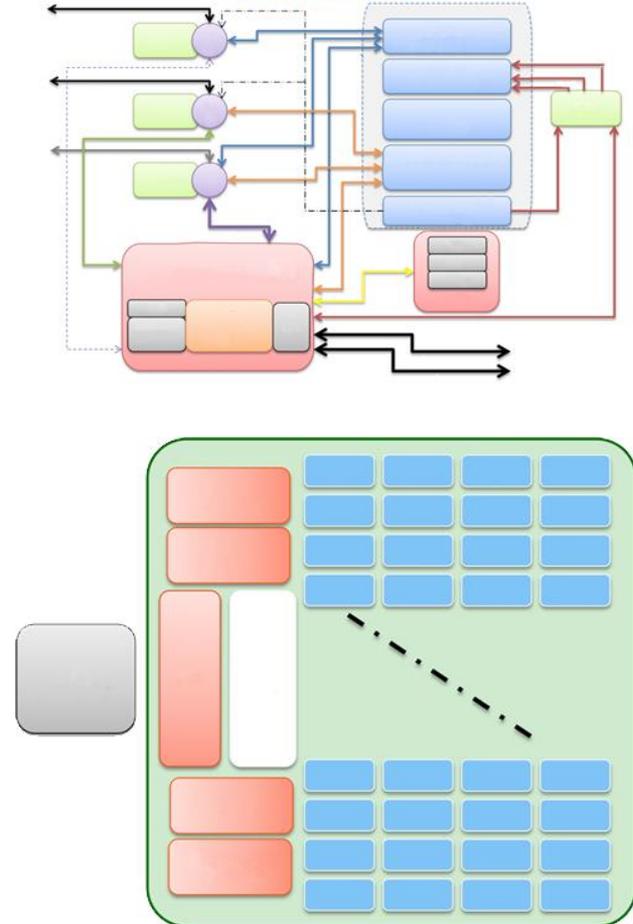
Intel's FFWD Elements

- RTL is implemented in an FPGA Emulator:
  - Enables hardware/software co-design by using a Hybrid Virtual Platform for emulation
  - Improves RTL validation coverage, including comprehensive fault resiliency analysis.
  - Allows performance estimation by running mini-apps on the emulator

- Alternate memory architectures and on-die interconnect topologies are explored:
  - Hierarchical and heterogeneous memory technologies
  - Various approaches to connect memories and cores on die

- Co-Design
  - The design is exercised in the simulator and the emulator through the porting and simulation of the six mini-applications LULESH, CoMD, miniFE, SMC, SNAP, Nekbone … and CLOMP

Hybrid Virtual Platform
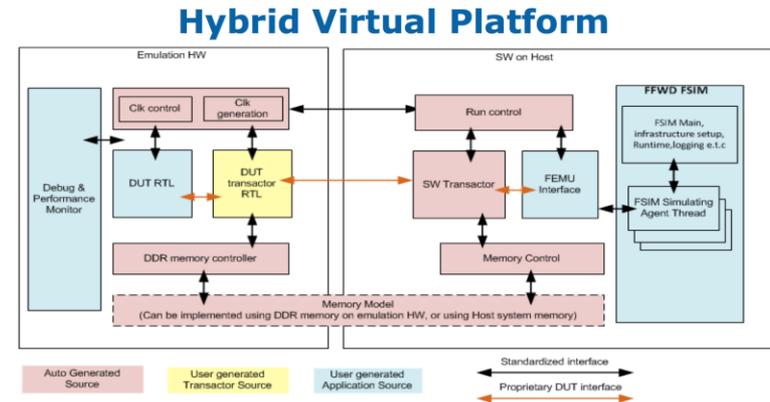
Memory and Network Interconnect
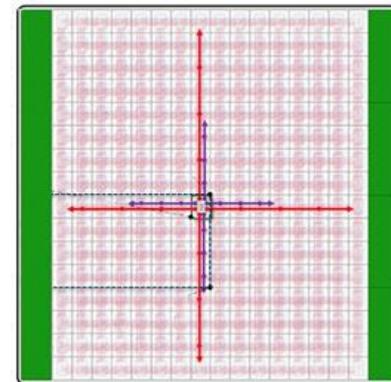
Co-design

- … has been very useful to us … (but we do receive mixed messages) ☺
  - We have adjusted the ISA and improved workload scaling
  - We are able to show the limits that the physical designs allow
  - Opened up the conversation to adjust "algorithmic thinking"
  - Open and honest dialog over MPI and OpenMP
- Hack-a-thons bring Labs together with Intel researchers
  - to exercise the design and alter it collaboratively
  - to alter the software stack and mini-apps
  - two sessions in 2013 and one in 2014 at an Intel facility with active Intel engineers in the room
    - Hands-on with internal simulators, tools

Summary

- First revision of next-gen Arch and models established
- NTV computations to reduce energy/op.
- Data movement limited by power and energy
  - Observed bandwidth tapers as the distance grows
- Data locality (programming system) is paramount
- Increase the on-die memory to compute ratio
- Rethink chip and chip design
  - Wires and transistors are cheap, feeding them expensive
- Sensors for introspection for dynamic resource management

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