# Edison (Ivy-Bridge):

- 12 Cores Per CPU
- 24 Virtual Cores Per CPU

- 2.4-3.2 GHz

- Can do 4 Double Precision Operations per Cycle (+ multiply/add)

- 2.5 GB of Memory Per Core

- ~100 GB/s Memory Bandwidth

Cori (Knights-Landing):

- Up to 72 Physical Cores Per CPU
- Up to 288 Virtual Cores Per CPU

- Lower GHz

- Can do 8 Double Precision Operations per Cycle (+ multiply/add)

- < 0.3 GB of HBM Memory Per Core
  < 2 GB of DDR Memory Per Core

- Fast memory has ~ 5x DDR4 bandwidth

Code Coverage

Breakdown of Application Hours on Hopper and Edison
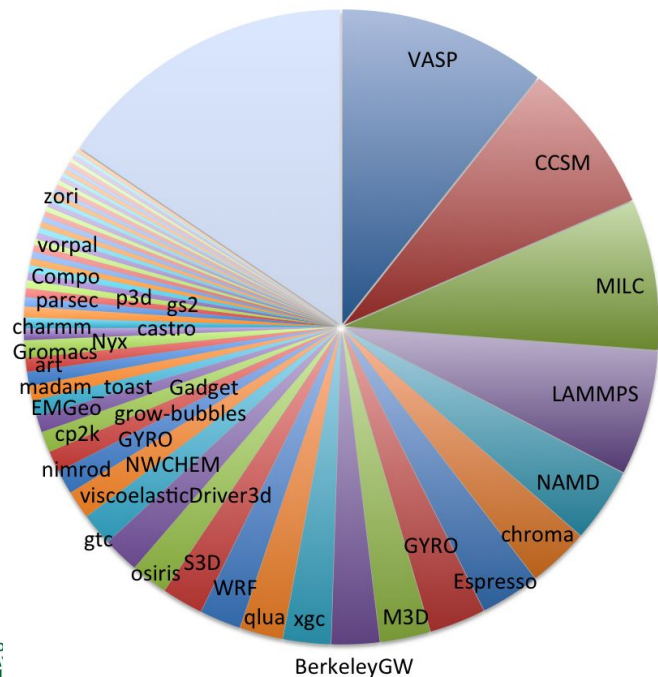
NESAP Tier-1, 2 Code

NESAP Proxy Code or Tier-3 Code
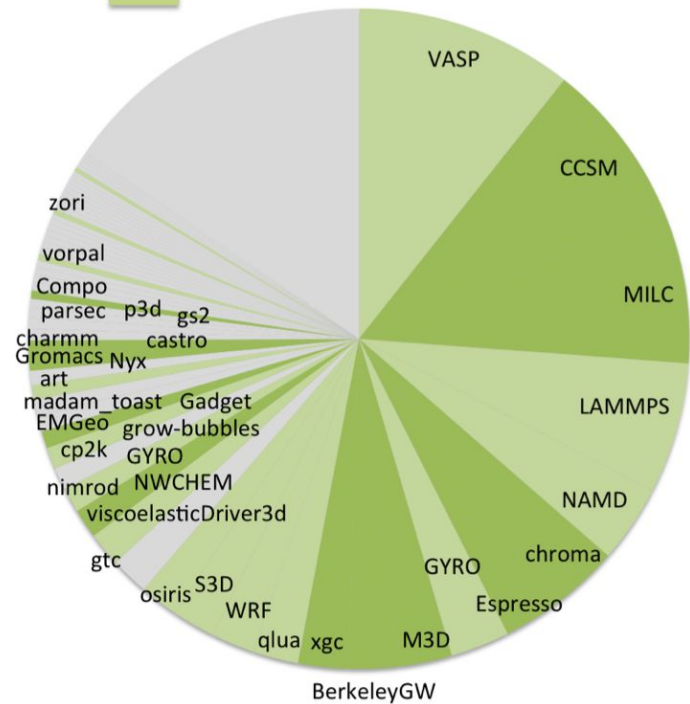
Resources for Code Teams

- **Early access to hardware**
  - Access to Babbage (KNC cluster) and early "white box" test systems expected in 2015
  - Early access and significant time on the full Cori system
- **Technical deep dives**
  - Access to Cray and Intel staff on-site staff for application optimization and performance analysis
  - Multi-day deep dive ('dungeon' session) with Intel staff at Oregon Campus to examine specific optimization issues
- **User Training Sessions**
  - From NERSC, Cray and Intel staff on OpenMP, vectorization, application profiling
  - Knights Landing architectural briefings from Intel
- **NERSC Staff as Code Team Liaisons (Hands on assistance)**
- **8 Postdocs**

NESAP Postdocs

Taylor Barnes
Quantum ESPRESSO

Brian Friesen
Boxlib

Andrey Ovsyannikov
Chombo-Crunch

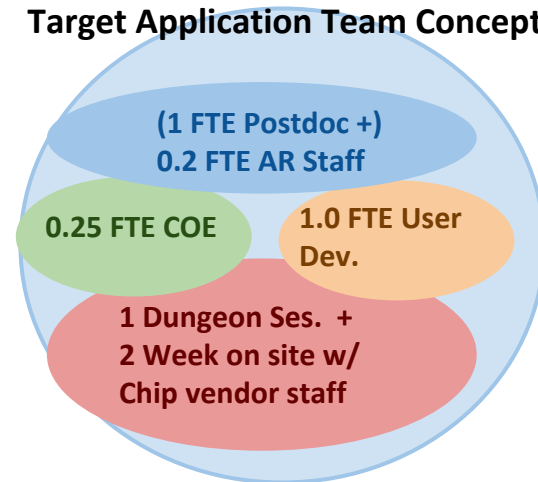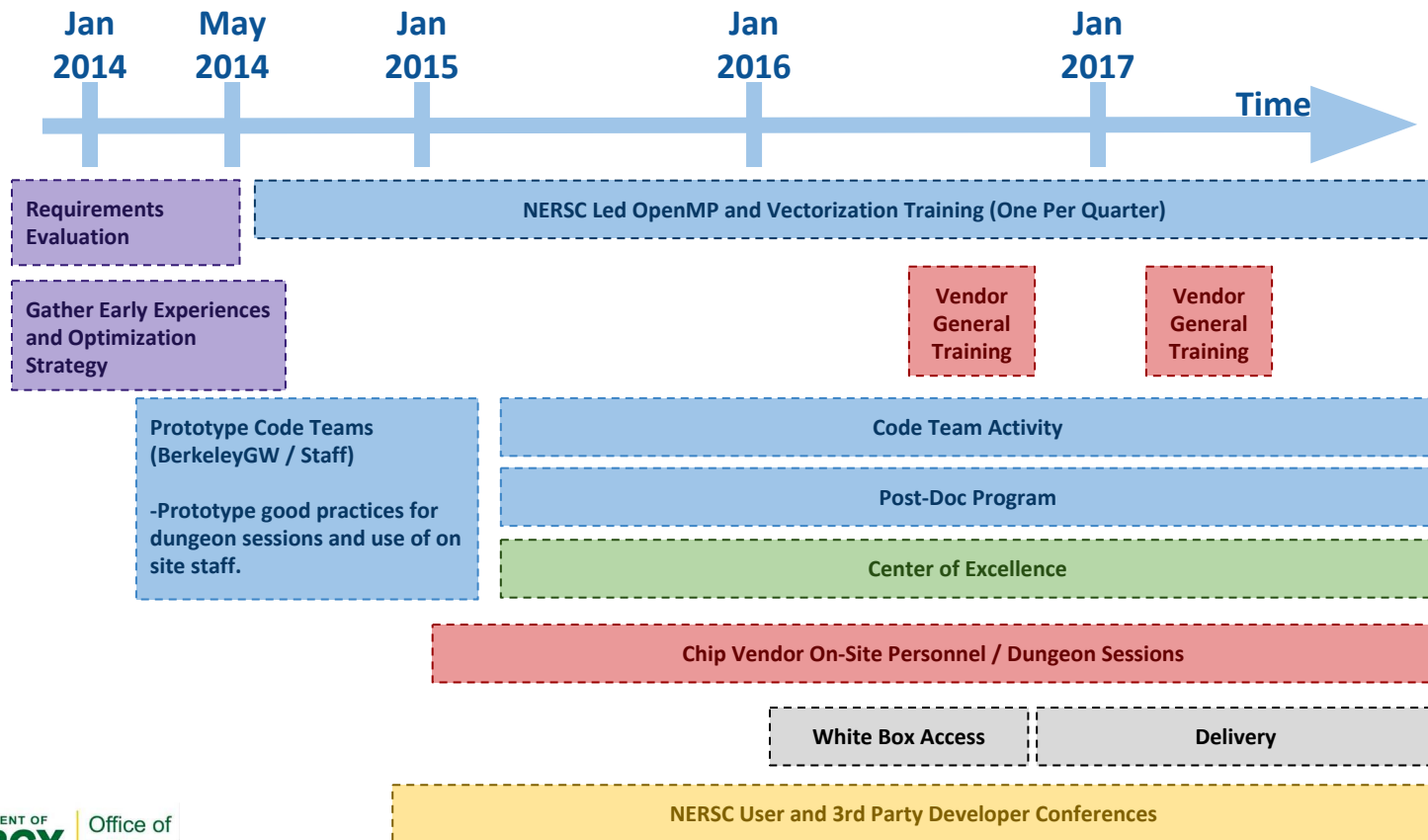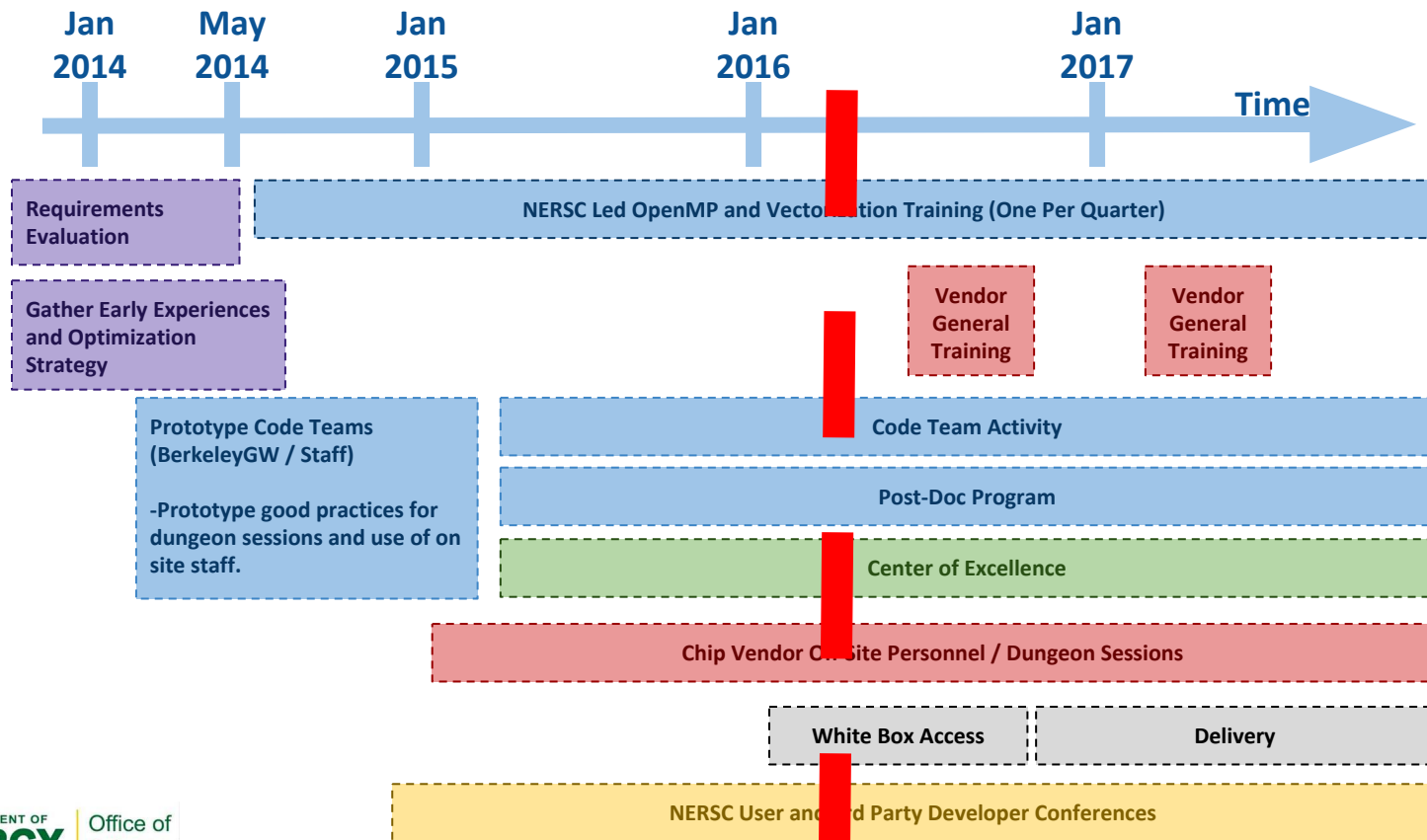Mathieu Lobet
WARP

Tuomas Koskela
XGC1

Tareq Malas
EMGeo

Target Application Team Concept

(1 FTE Postdoc +) 0.2 FTE AR Staff

0.25 FTE COE

1.0 FTE User Dev.

1 Dungeon Ses. + 2 Week on site w/ Chip vendor staff

Timeline

Jan 2014   May 2014   Jan 2015   Jan 2016   Jan 2017 → **Time**

- **Requirements Evaluation**
- **NERSC Led OpenMP and Vectorization Training (One Per Quarter)**
- **Gather Early Experiences and Optimization Strategy**
- **Vendor General Training**
- **Vendor General Training**
- **Prototype Code Teams (BerkeleyGW / Staff)**

  -Prototype good practices for dungeon sessions and use of on site staff.
- **Code Team Activity**
- **Post-Doc Program**
- **Center of Excellence**
- **Chip Vendor On-Site Personnel / Dungeon Sessions**
- **White Box Access**
- **Delivery**
- **NERSC User and 3rd Party Developer Conferences**

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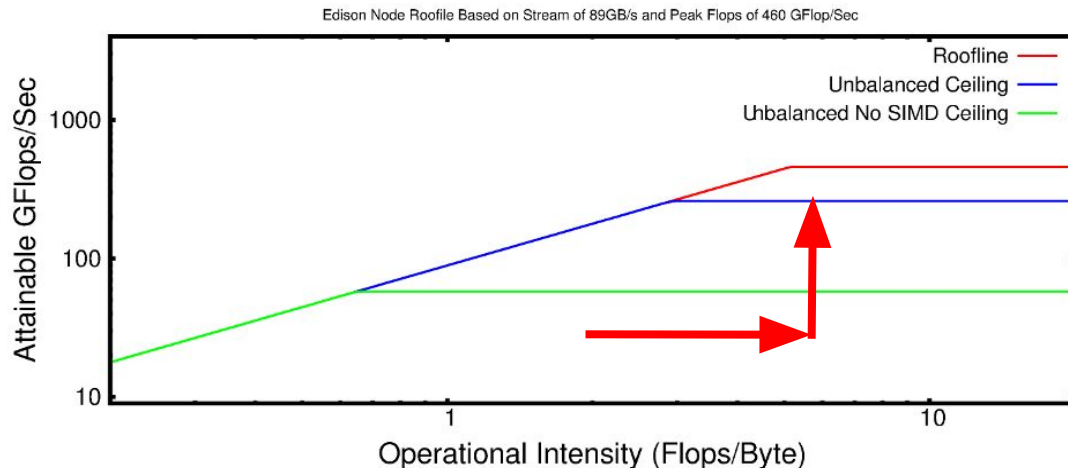
Important Optimization Concepts

- **MPI+X (Where X is MPI, OpenMP, PThreads, PGAS etc)**

- **Understanding Memory Bandwidth**

- **Vectorization**

Edison Node Roofile Based on Stream of 89GB/s and Peak Flops of 460 GFlop/Sec

Roofline
Unbalanced Ceiling
Unbalanced No SIMD Ceiling

Attainable GFlops/Sec

Operational Intensity (Flops/Byte)

The Ant Farm!

OpenMP scales only to 4 Threads

large cache miss rate

Code shows no improvements when turning on vectorization

50% Walltime is IO

Compute intensive doesn't vectorize

Communication dominates beyond 100 nodes

Memory bandwidth bound kernel

IO bottlenecks

MPI/OpenMP Scaling Issue

Can you use a library?

Increase Memory Locality

Utilize High-Level IO-Libraries. Consult with NERSC about use of Burst Buffer.

Use Edison to Test/Add OpenMP Improve Scalability. Help from NERSC/Cray COE Available.

Create micro-kernels or examples to examine thread level performance, vectorization, cache use, locality.

Utilize performant / portable libraries

The Dungeon: Simulate kernels on KNL. Plan use of on package memory, vector instructions.

# Dungeon Prep Flow Chart

The Ant Farm Flow Chart
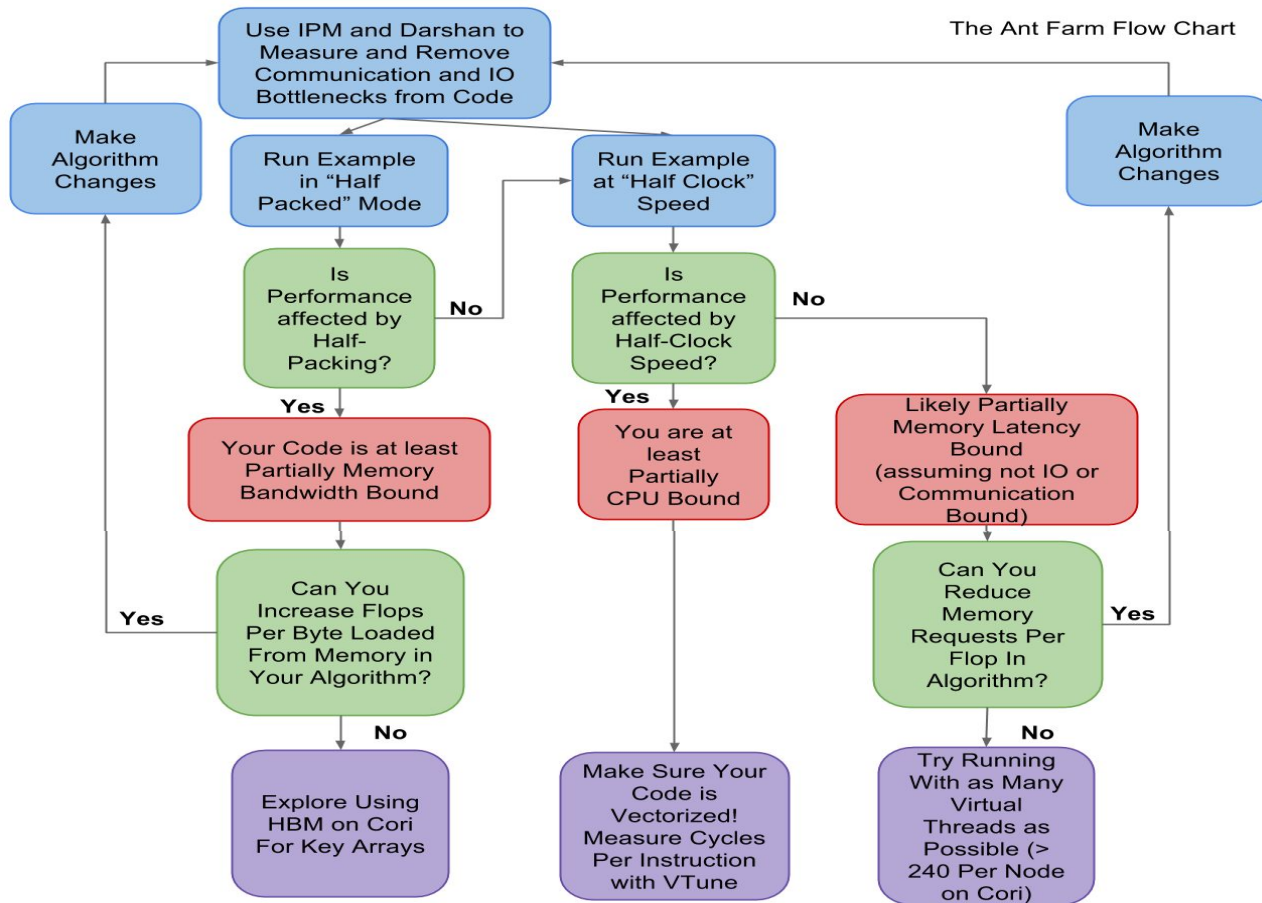
What Has Gone Well

1. Setting requirements for Dungeon Session motivates teams to get started early and improves quality of dungeon session.
2. Engagement with IXPUG and user communities (Exascale Workshops at CRT)
3. Large number of NERSC and Vendor Training (Vectorization, OpenMP, Tools/Compilers)
4. Learned a Lot about Tools and Architecture (VTune, SDE, HBM, Crapat, Reveal etc.)
5. Vendors Keen to Help

Warp Vectorization Improvements at The Dungeon - Directly enabled by tiling work with Cray COE in Pre-dungeon

Tiling improves memory locality

Loop Vectorization
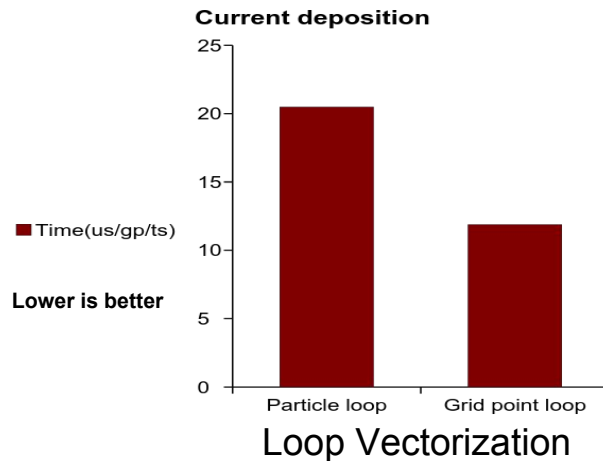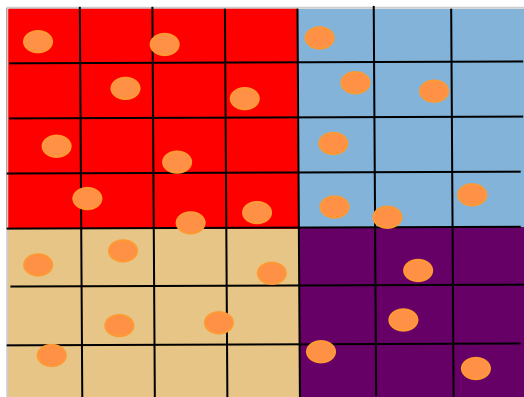
What Our Users Want

- Performance - They want to do as much science possible on the largest/most-impactful systems they can

- Portability - They run on multiple systems in the DOE and elsewhere. Where possible want fewer branches.

- Continuity - They want to know investments they make now won't have to be remade every two years.

Extras

NERSC Staff associated with NESAP

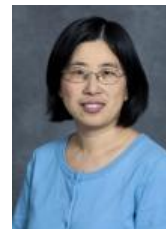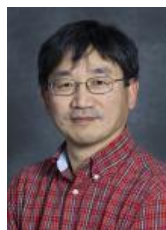Katie Antypas   Nick Wright   Richard Gerber   Brian Austin   Zhengji Zhao   Helen He   Ankit Bhagatwala   Stephen Leak

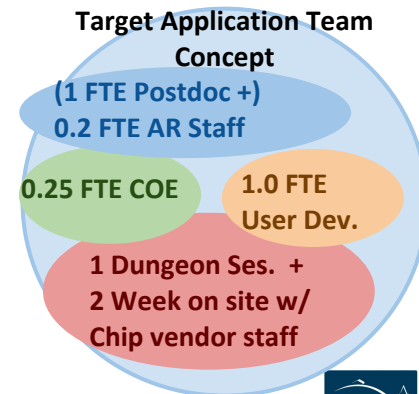Woo-Sun Yang   Rebecca Hartman-Baker   Doug Doerfler   Jack Deslippe   Brandon Cook   Thorsten Kurth

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Working With Vendors

NERSC and other centers are uniquely positioned between HPC Vendors and HPC Users and Applications developers.

NESAP provides a power venue for these two groups to interact.

Dungeon Session Speedups (From Session Itself)